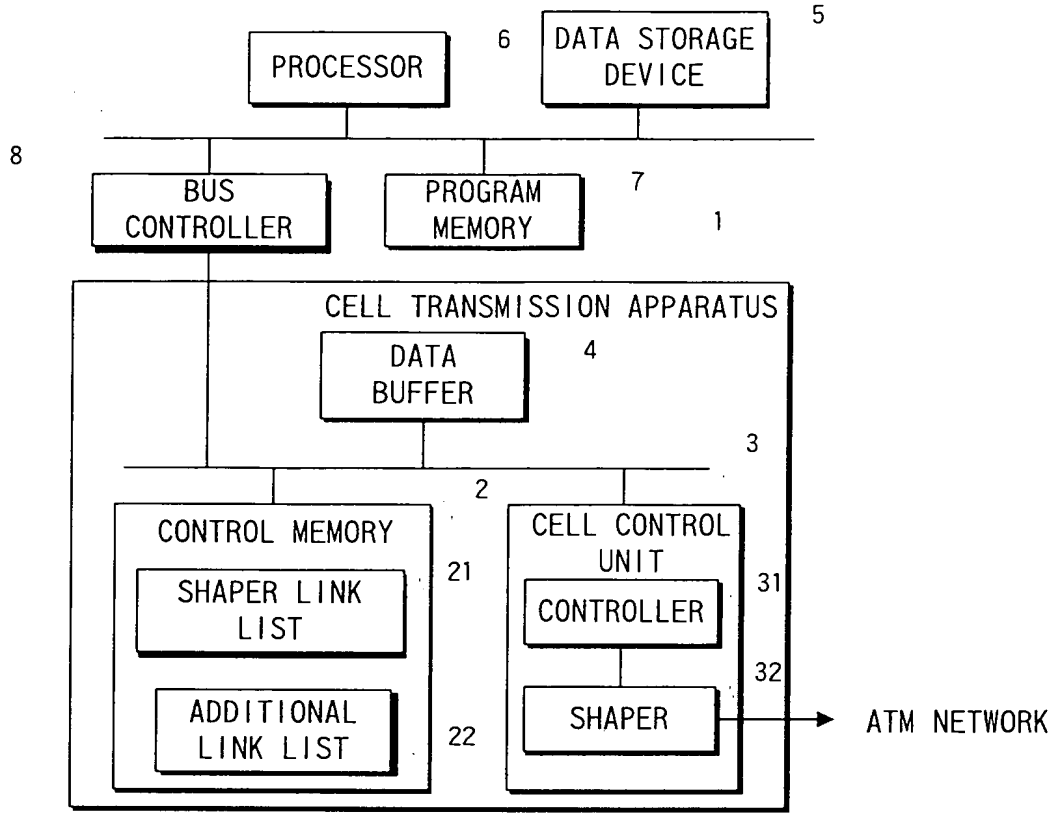

PROCESSOR
6
DATA STORAGE DEVICE
5
8
BUS CONTROLLER
PROGRAM MEMORY
7
1
CELL TRANSMISSION APPARATUS
DATA BUFFER
4
3
2
CONTROL MEMORY
SHAPER LINK LIST
21
ADDITIONAL LINK LIST
22
CELL CONTROL UNIT
CONTROLLER
31
32
SHAPER
ATM NETWORK

FIG. 1

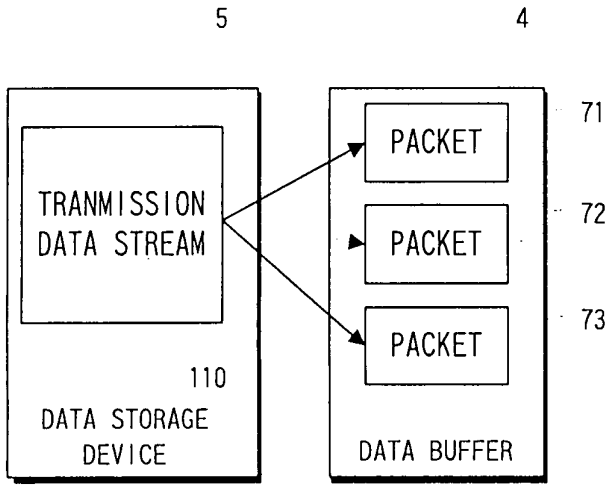

5
4
TRANMISSION DATA STREAM
110
DATA STORAGE DEVICE
PACKET
PACKET
PACKET
71
72
73
DATA BUFFER

FIG. 2a

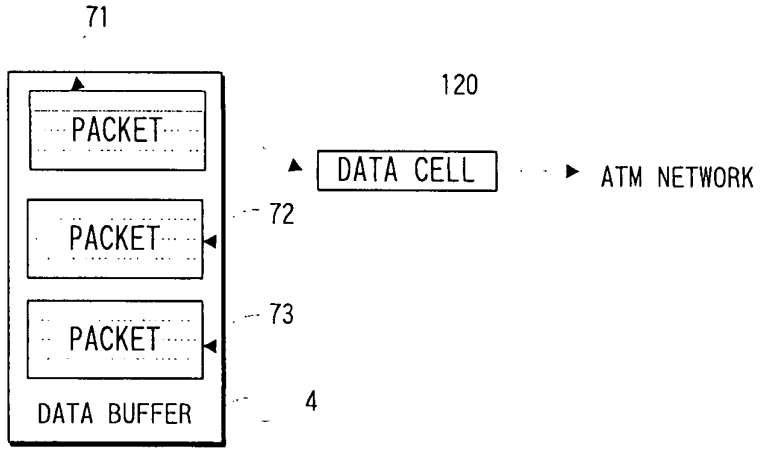
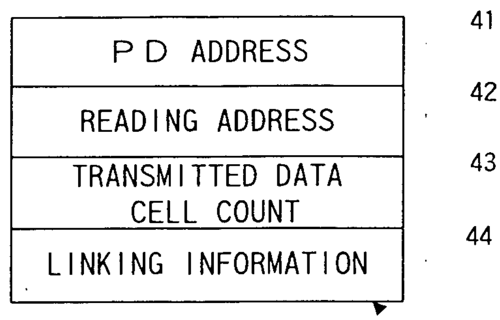

71
PACKET
PACKET
PACKET
72
73
DATA BUFFER
4
120
DATA CELL
ATM NETWORK

FIG. 2b



VC INFORMATION 40

FIG.3

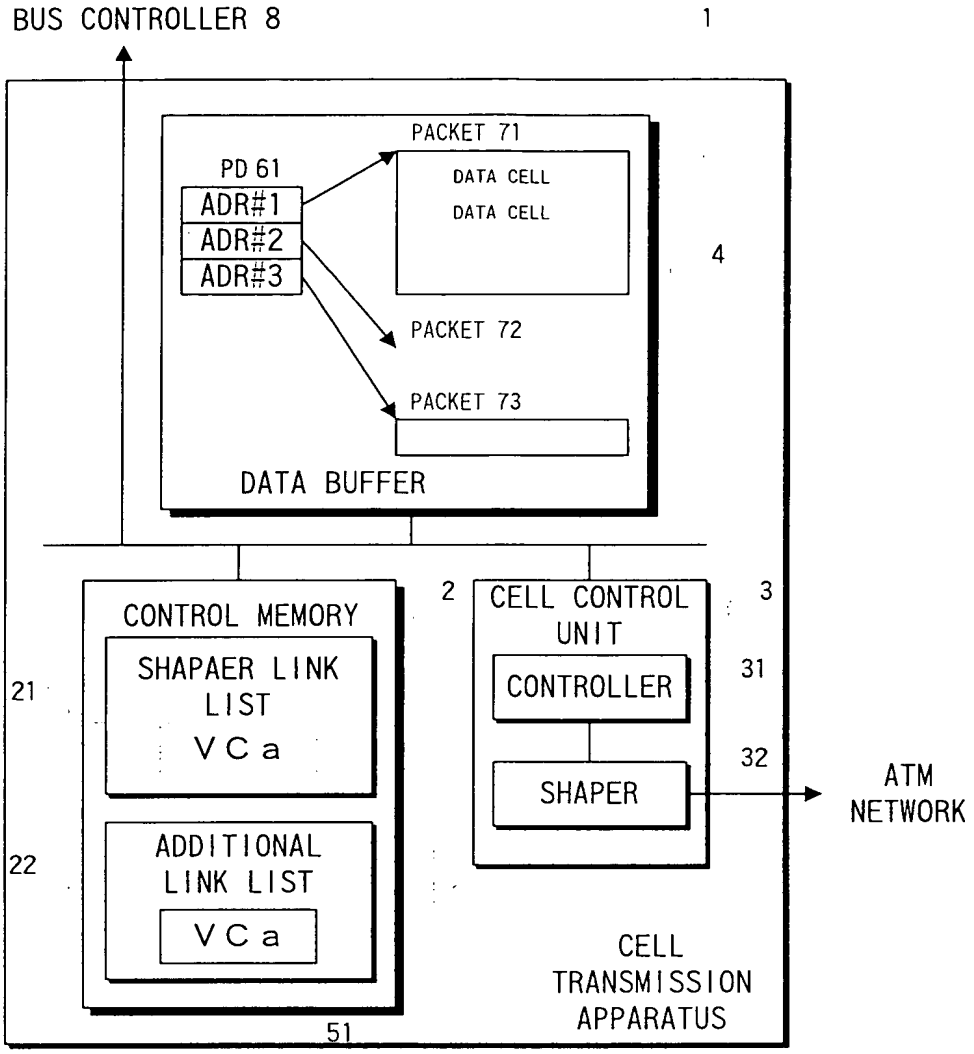

BUS CONTROLLER 8
1
PACKET 71
PD 61
ADR#1
ADR#2
ADR#3
DATA CELL
DATA CELL
4
PACKET 72
PACKET 73
DATA BUFFER
2
CONTROL MEMORY
21
SHAPAER LINK LIST
VCa
22
ADDITIONAL LINK LIST
VCa
51
3
CELL CONTROL UNIT
31
CONTROLLER
32
SHAPER
ATM NETWORK
CELL TRANSMISSION APPARATUS

FIG. 4

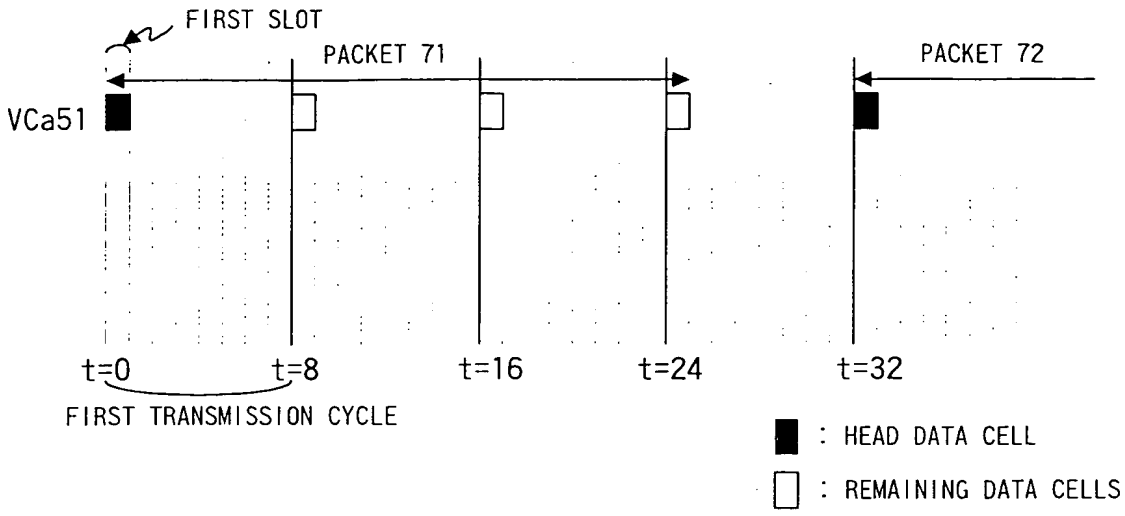

FIRST SLOT
PACKET 71
PACKET 72
VCa51
t=0
t=8
t=16
t=24
t=32
FIRST TRANSMISSION CYCLE
: HEAD DATA CELL
: REMAINING DATA CELLS

FIG. 5

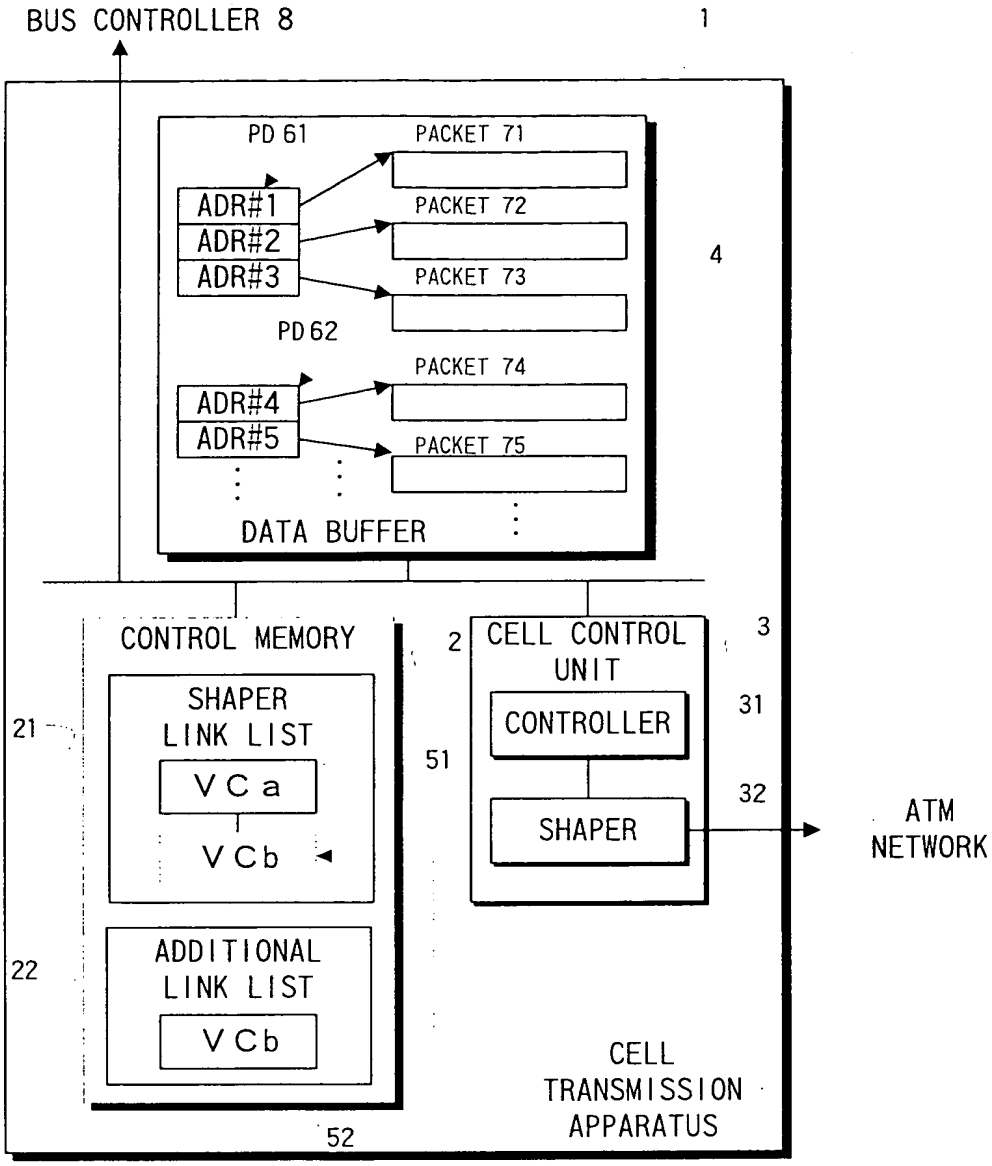

BUS CONTROLLER 8
1
PD 61
PACKET 71
ADR#1
PACKET 72
ADR#2
ADR#3
PACKET 73
4
PD 62
PACKET 74
ADR#4
ADR#5
PACKET 75
DATA BUFFER
CONTROL MEMORY
2
CELL CONTROL UNIT
3
SHAPER LINK LIST
21
CONTROLLER
31
VCa
51
VCb
32
SHAPER
ATM NETWORK
ADDITIONAL LINK LIST
22
VCb
CELL TRANSMISSION APPARATUS
52

FIG. 6

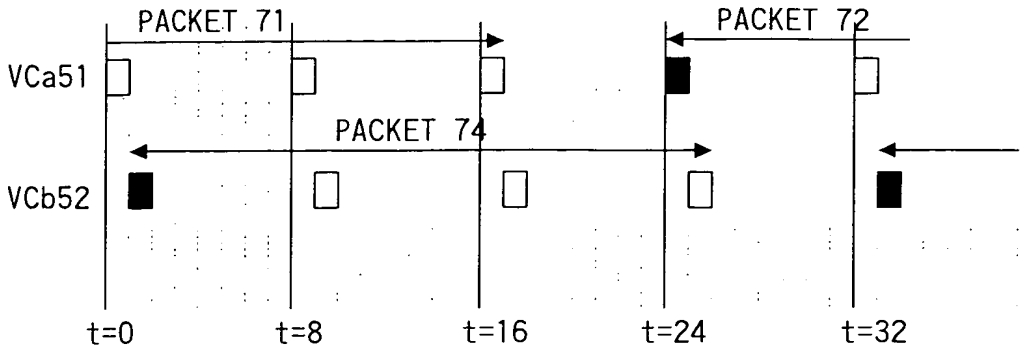

PACKET 71
PACKET 72
VCa51
PACKET 74
VCb52
t=0
t=8
t=16
t=24
t=32

FIG. 7a

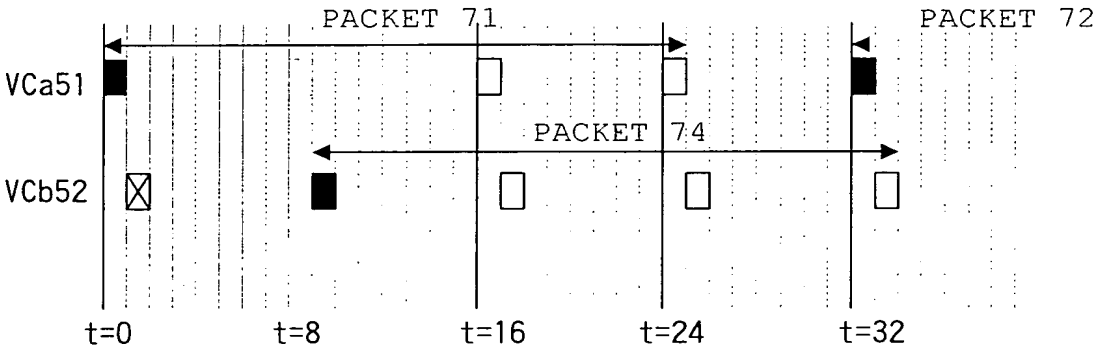

PACKET 71
PACKET 72
VCa51
PACKET 74
VCb52
t=0
t=8
t=16
t=24
t=32

FIG. 7b

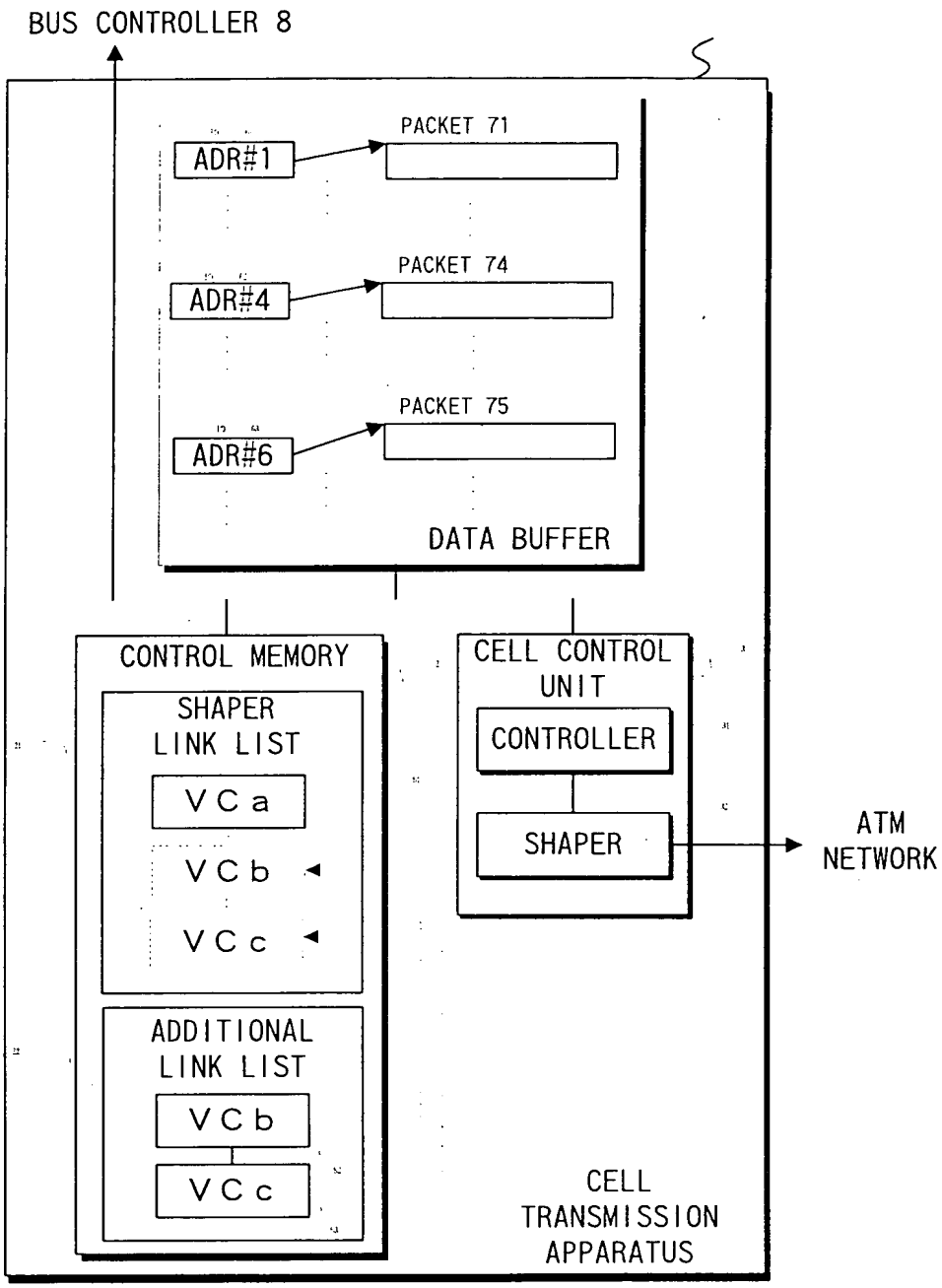

BUS CONTROLLER 8
5
PACKET 71
ADR#1
PACKET 74
ADR#4
PACKET 75
ADR#6
DATA BUFFER
CONTROL MEMORY
SHAPER
LINK LIST
VCa
VCb
VCc
ADDITIONAL
LINK LIST
VCb
VCc
CELL CONTROL
UNIT
CONTROLLER
SHAPER
ATM
NETWORK
CELL
TRANSMISSION
APPARATUS

FIG. 8

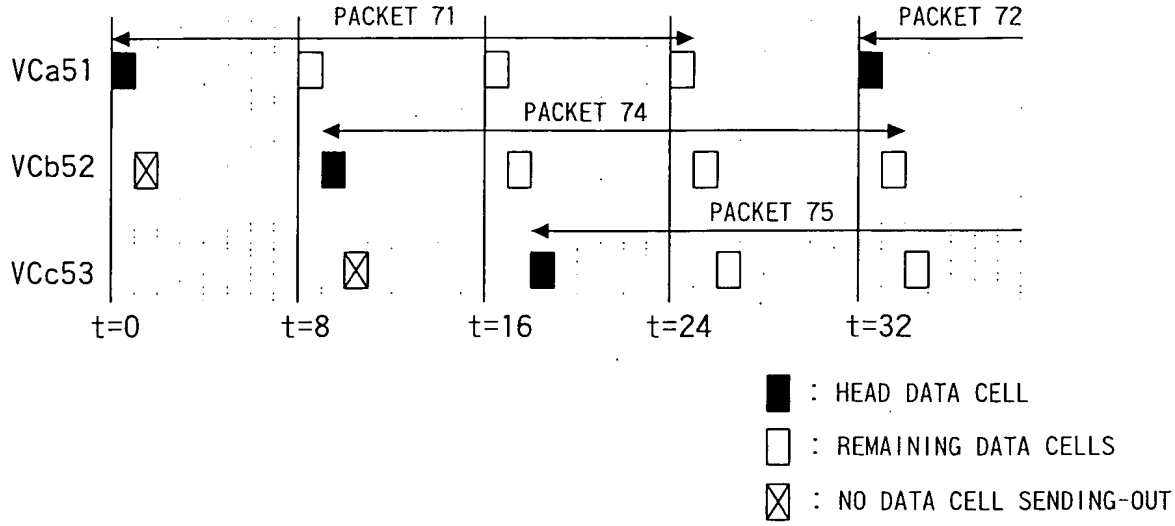

PACKET 71
PACKET 72
VCa51
PACKET 74
VCb52
PACKET 75
VCc53
t=0
t=8
t=16
t=24
t=32
: HEAD DATA CELL
: REMAINING DATA CELLS
: NO DATA CELL SENDING-OUT

FIG. 9a

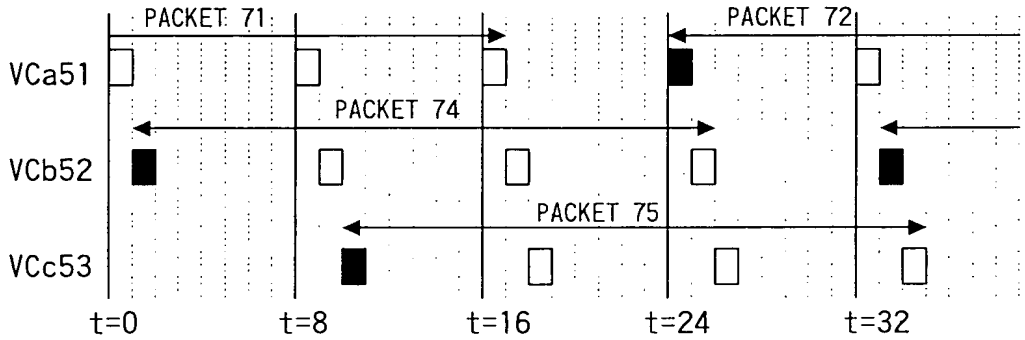

PACKET 71
PACKET 72
VCa51
PACKET 74
VCb52
PACKET 75
VCc53
t=0
t=8
t=16
t=24
t=32

FIG. 9b

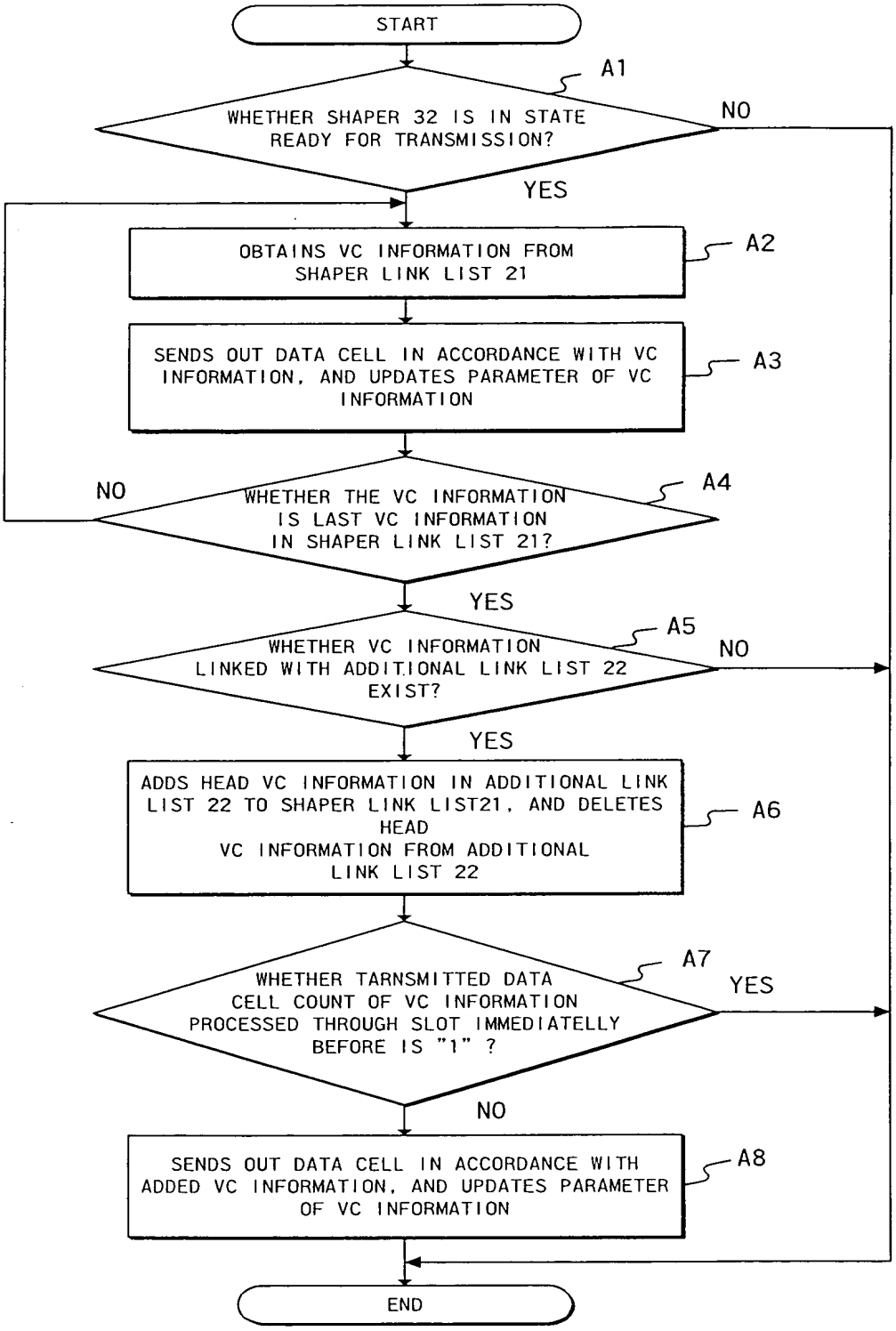

START
A1
WHETHER SHAPER 32 IS IN STATE READY FOR TRANSMISSION?
NO
YES
OBTAINS VC INFORMATION FROM SHAPER LINK LIST 21
A2
SENDS OUT DATA CELL IN ACCORDANCE WITH VC INFORMATION, AND UPDATES PARAMETER OF VC INFORMATION
A3
NO
WHETHER THE VC INFORMATION IS LAST VC INFORMATION IN SHAPER LINK LIST 21?
A4
YES
WHETHER VC INFORMATION LINKED WITH ADDITIONAL LINK LIST 22 EXIST?
A5
NO
YES
ADDS HEAD VC INFORMATION IN ADDITIONAL LINK LIST 22 TO SHAPER LINK LIST21, AND DELETES HEAD VC INFORMATION FROM ADDITIONAL LINK LIST 22
A6
WHETHER TARNSMITTED DATA CELL COUNT OF VC INFORMATION PROCESSED THROUGH SLOT IMMEDIATELLY BEFORE IS "1" ?
A7
YES
NO
SENDS OUT DATA CELL IN ACCORDANCE WITH ADDED VC INFORMATION, AND UPDATES PARAMETER OF VC INFORMATION
A8
END

FIG. 10

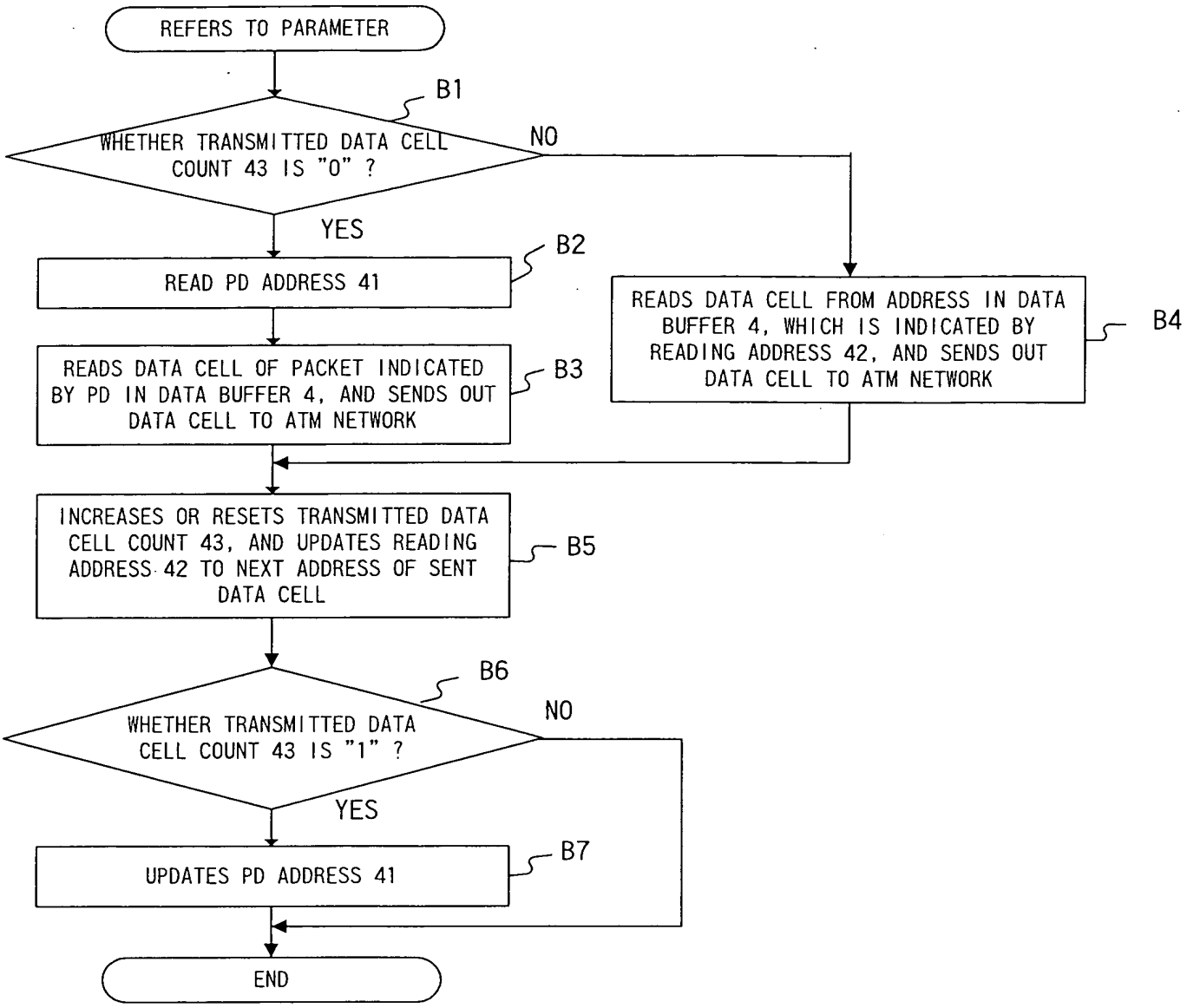

REFERS TO PARAMETER
B1
WHETHER TRANSMITTED DATA CELL COUNT 43 IS "0" ?
NO
YES
B2
READ PD ADDRESS 41
READS DATA CELL OF PACKET INDICATED BY PD IN DATA BUFFER 4, AND SENDS OUT DATA CELL TO ATM NETWORK
B3
READS DATA CELL FROM ADDRESS IN DATA BUFFER 4, WHICH IS INDICATED BY READING ADDRESS 42, AND SENDS OUT DATA CELL TO ATM NETWORK
B4
INCREASES OR RESETS TRANSMITTED DATA CELL COUNT 43, AND UPDATES READING ADDRESS 42 TO NEXT ADDRESS OF SENT DATA CELL
B5
B6
WHETHER TRANSMITTED DATA CELL COUNT 43 IS "1" ?
NO
YES
B7
UPDATES PD ADDRESS 41
END

FIG. 11